CLAIMS

What is claimed is:

1. A method comprising:

receiving a software program having a plurality of instructions; and

performing instrumentation on the software program to determine a plurality of addresses of the plurality of instructions of the software program in the order in which the plurality of instructions are executed by a processor.

2. The method of claim 1, wherein performing instrumentation on the software program comprises inserting an instrumentation source block (ISB) before one or more instructions of the plurality of instructions to determine one or more address of the one or more instructions in the software program.

3. The method of claim 2, further comprising providing an offset to the ISB to remove a skew in the one or more addresses caused by performing instrumentation on the software program.

4. The method of claim 2, wherein performing instrumentation on the software program further comprises inserting a plurality of store instructions before the ISB to store content of a plurality of registers of the processor and a plurality of restore instructions after the ISB to restore the content of the plurality of registers of the processor.

5. The method of claim 1, wherein the plurality of instructions in the software program are discretely identifiable.

6. The method of claim 1, wherein one or more of the plurality of instructions in the software program are not discretely identifiable.

7. The method of claim 6, further comprising converting the software program into a format where the plurality of instructions are discretely identifiable.

8. The method of claim 2, wherein the ISB includes instructions to output one or more instruction addresses.

9. The method of claim 2, wherein the ISB includes a branch instruction to branch to a routine which comprises one or more instructions to output one or more of the plurality of addresses.

10. The method of claim 9, further comprising:

appending a binary file of the output routine to a plurality of binary files of the software program; and

providing the plurality of binary files of the software program with the binary file of the output routine to a linker.

11. A machine-readable medium embodying codes, the codes, when executed by a processor, causing the processor to perform a plurality of operations, the plurality of operations comprising:

receiving a software program having a plurality of instructions; and

performing instrumentation on the software program to determine a plurality of addresses of the plurality of instructions of the software program in the order in which the plurality of instructions are executed by a processor.

12. The machine-readable medium of claim 11, wherein performing instrumentation on the software program comprises inserting an instrumentation source block (ISB) before one or more instructions of the plurality of instructions to determine one or more address of the one or more instructions in the software program.

13. The machine-readable medium of claim 12, wherein performing instrumentation on the software program further comprises providing an offset to the ISB to remove a skew in the one or more address caused by instrumentation of the software program.

14. The machine-readable medium of claim 12, wherein instrumentation of the software program further comprises inserting a plurality of store instructions before the ISB to store content of a plurality of registers of the processor and a plurality of restore instructions after the ISB to restore the content of the plurality of registers of the processor.

15. A system comprising:

a processor; and

a dynamic random access memory ("DRAM") device to store a first computer program, the first computer program including a first plurality of instructions, which when executed by a processor, causes the processor to perform a plurality of operations on a second computer program, the plurality of operations comprising

receiving the second computer program, the second computer program having a second plurality of instructions; and

performing instrumentation on the second computer program to determine a plurality of addresses of the second plurality of instructions of the second computer program in the order in which the second plurality of instructions are executed by the processor.

16. The system of claim 15, wherein performing instrumentation on the second computer program comprises inserting an instrumentation source block (ISB) before one or more instruction of the second plurality of instructions to determine one or more address of the one or more instruction in the second computer program.

17. The system of claim 16, wherein performing instrumentation on the second computer program further comprises providing an offset to the ISB to remove a skew in the one or more address caused by performing instrumentation on the second computer program.

18. The system of claim 16, wherein performing instrumentation on the second computer program further comprises inserting a plurality of store instructions before the ISB to store content of a plurality of registers of the processor and a plurality of restore instructions after the ISB to restore the content of the plurality of registers of the processor.

19. The system of claim 15, wherein the second plurality of instructions in the second computer program are discretely identifiable.

20. The system of claim 15, wherein the second plurality of instructions in the second computer program are not discretely identifiable.

21. The system of claim 20, wherein the plurality of operations comprises converting the second computer program into a format in which the second plurality of instructions are discretely identifiable.

22. The system of claim 16, wherein the ISB includes instructions to output the one or more address of the one or more instruction in the second computer program.

23. The system of claim 16, wherein the ISB includes a branch instruction to branch to a routine which includes one or more instructions to output the one or more address of the one or more instruction in the second computer program.